partial layer having a first dopant concentration disposed on a second partial layer having a second dopant concentration, the second dopant concentration being less than the first dopant concentration; and

a second layer of a second conductivity type which is opposite of the first conductivity type, wherein the second layer is disposed on the first partial layer;

wherein at least one trench is provided such that the trench penetrates the first partial layer and extends into the second partial layer, and wherein the trench is covered by a continuation region of the second layer so that at least one p-n junction is provided between the second layer and the second partial layer of the chip.

9. (New) The semiconductor chip according to claim 8, wherein an edge region of the chip is beveled, and wherein additional continuation regions of the second layer are provided in the edge region to form additional p-n junctions in combination with the second partial layer.

A' cont.

10. (New) The semiconductor chip according to claim 8, wherein a third partial layer connected to the second partial layer is provided.

11. (New) A method for manufacturing a semiconductor chip, comprising the steps of:

providing a semiconductor wafer which includes a first layer having at least two partial layers, the first partial layer being disposed on the second partial layer, the two partial layers having a first conductivity type, the first partial layer having a first dopant concentration, the second partial layer having a second dopant concentration, and the second dopant concentration being less than the first dopant concentration;

introducing trenches into the first partial layer, which trenches extend through the first partial layer into the second partial layer;

introducing dopants of a second conductivity type into the top surface of the